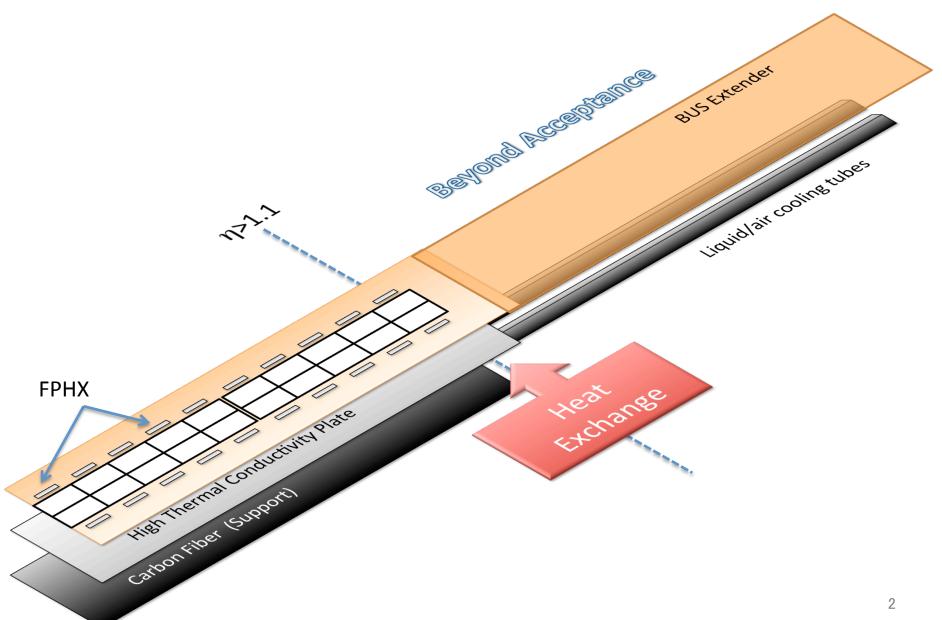
INTT Material Budget Plan

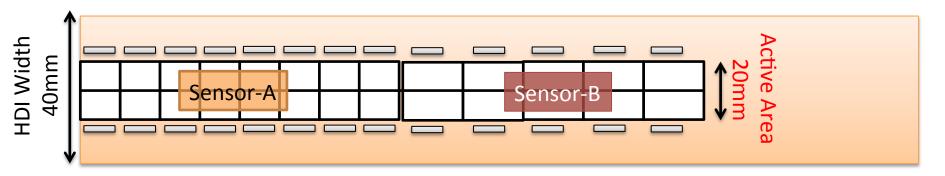
RIKEN/RBRC
Itaru Nakagawa

Ladder Structure

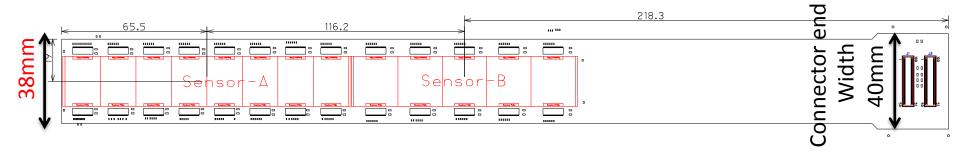


Silicon Module

Present INTT GEANT Model

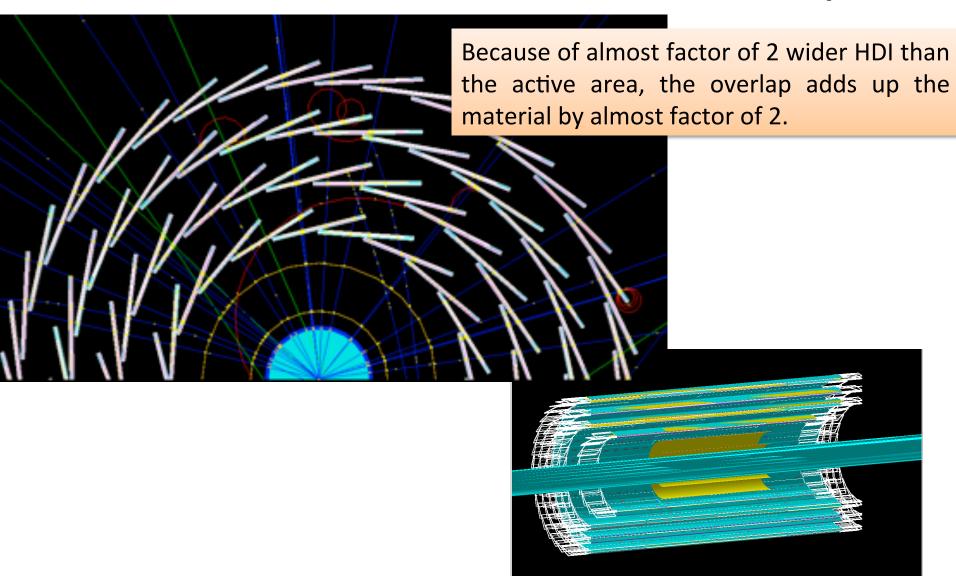


Prototype Design



The 38mm is the technological limit width. It is unlikely this width becomes narrower in the future R&D.

INTT Barrel and Ladder Overlap

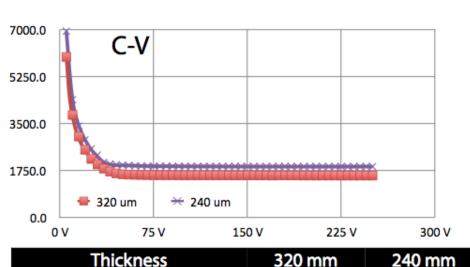


INTT Ladder Material Budget

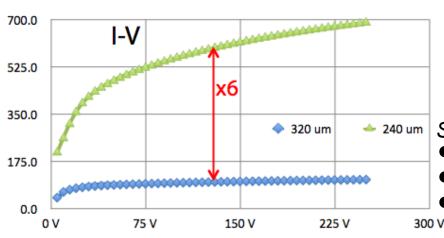
| | Thickness | Radiation Length X/X ₀ | R & D Goal |
|------------------------------------|-----------|-----------------------------------|----------------|
| Silicon | 240 μm | 0.3 % | 0.25 ~ 0.3 % |
| HDI | < 500 μm | 0.7 % | 0.34 ~ 0.7% |
| High Thermal Conductivity Plate | 350 μm | 0.18 % | 0.09? ~ 0.18 % |
| Carbon Fiber Support | 230 μm | 0.08 % | 0.05? ~ 0.08% |
| Total | | 1.26 % | 0.73? ~ 1.26% |

X/X0 is multiplied by 2 for overlapping ladder

Reducing Material (Silicon sensors)



| Thickness | 320 mm | 240 mm |
|----------------------------|--------|--------|
| Full Depletion Voltage [V] | 45 | < 45 |





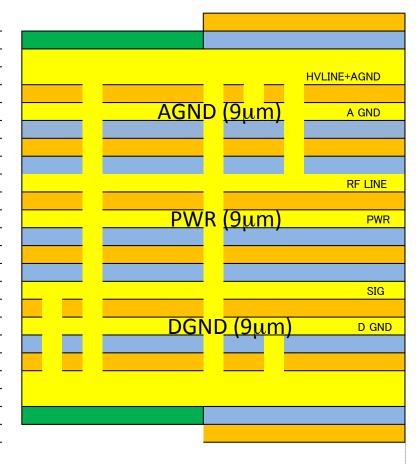
| Thickness | 200 μm | 240 μm | 320 μm |
|-------------------------|-----------------------|----------|----------|
| X0 | 0.21% | 0.26% | 0.34% |
| Dark current / 320μm | similar with 240μm | x6 | x1 |
| Price | > 0.5k USD? | 0.4k USD | 0.3k USD |

Silicon sensors for the strip layers

- Two thicknesses, 240 μm and 320 μm.
- 240 μm sensor is made by grinding 320 μm one.
- Hamamatsu says 200 μm is possible.
 - → compromise with increasing dark current.

HDI Layer Structure

| | Regist | 20 μ m |
|----|-------------------------|----------|
| | Copper plated | 15 μ m |
| L1 | Electrolytic copper foi | 9 μ m |
| | Base Polyimide | 50 μm |
| L2 | Electrolytic copper foi | 9 μ m |
| | Glue | 15 |
| | Coverlay Polymide | 12.5 μm |
| | Glue | 25 μ m |
| L3 | Electrolytic copper foi | 9 μ m |
| | Base Polyimide | 50 μ m |
| L4 | Electrolytic copper foi | 9 μ m |
| | Glue | 15 μ m |
| | Coverlay Polymide | 12.5 μ m |
| | Glue | 25 μ m |
| L5 | Electrolytic copper foi | 9 μ m |
| | Base Polyimide | 25 μ m |
| L6 | Electrolytic copper foi | 9 μ m |
| | Bonding Sheet | 25 μ m |
| | Base Polyimide | 50 μ m |
| L7 | Electrolytic copper foi | 9 μ m |
| | Copper plated | 15 μ m |
| | Regist | 20 μ m |
| | | μm |
| | | |



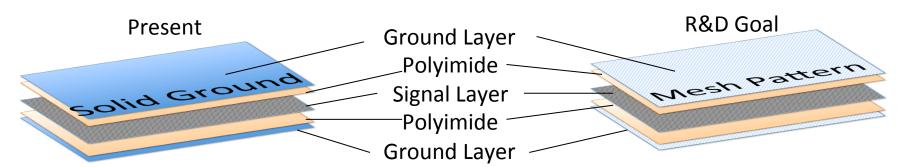
| Coverlay Polyimide | 12.5 μm |
|--------------------------|--|
| Coverlay Glue | 25 μm |
| Copper plated | 15 μ m |
| Electrolytic copper foil | 9 μ m |
| Base Polyimide | 50 μm |
| Electrolytic copper foil | 9 μ m |
| Glue | 15 μ m |
| Coverlay Polyimide | 12.5 μm |
| Glue | 25 μ m |
| Electrolytic copper foil | 9 μ m |
| Base Polyimide | 50 μm |
| Electrolytic copper foil | 9 μ m |
| Glue | 15 μ m |
| Coverlay Polyimide | 12.5 μ m |
| Glue | 25 μ m |
| Electrolytic copper foil | 9 μ m |
| Base Polyimide | 25 μ m |
| Electrolytic copper foil | 9 μ m |
| Bonding Sheet | 25 μ m |
| Base Polyimide | 50 μ m |
| Electrolytic copper foil | 9 μ m |
| Copper plated | 15 |
| Coverlay Glue | 25 μ m |
| Coverlay Polyimide | 12.5 μ m |
| | Coverlay Glue Copper plated Electrolytic copper foil Base Polyimide Electrolytic copper foil Glue Coverlay Polyimide Glue Electrolytic copper foil Base Polyimide Electrolytic copper foil Glue Coverlay Polyimide Electrolytic copper foil Glue Coverlay Polyimide Electrolytic copper foil Base Polyimide Electrolytic copper foil Base Polyimide Electrolytic copper foil Bonding Sheet Base Polyimide Electrolytic copper foil Copper plated Coverlay Glue |

438 μm

TOTAL/Thickness 473 μ m

| TOTAL Thickness | Material | X/X _o | R&D Goal |
|-----------------|--------------------|------------------|----------|
| TOTAL, MICKIESS | Polyimide Total | 0.3 % | |
| | Cupper Layer Total | 0.4 % | |

Reducing Material (HDI)



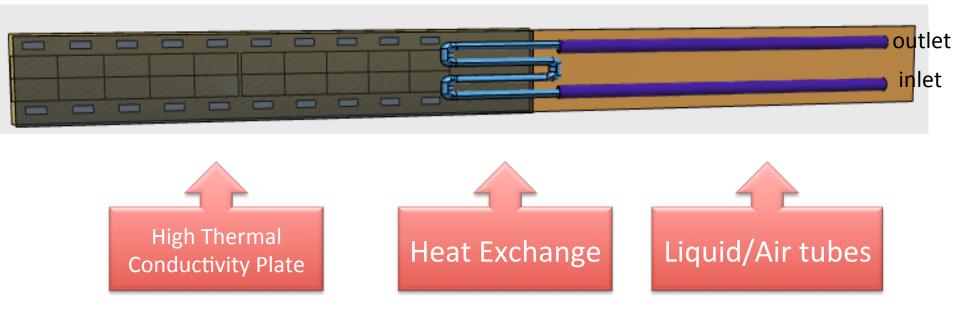
Signal layers are electrically shielded by sandwiched by solid ground layers

solid ground layers are meshed pattern so that to reduce material without loosing noise shielding performance. The goal is to reduce the Cu material by 10%. (Prototype is to be delivered in April)

| Material | X/X _o | R&D Goal |
|--------------------|------------------|----------|
| Polyimide Total | 0.3 % | |
| Cupper Layer Total | 0.4 % | 0.04 % |

Reducing Material: High Thermal Conductivity Plate

View from the back



The point of high thermal conductivity plate is to transport the heat from the chip to the heat exchange. Carbon fiber support is not drawn here for visibility.

Cooling Option

 In addition to air cooling option, the high thermal conductivity plate (sheet) will be tested. It has an advantage to make the cooling system even simpler and less material.

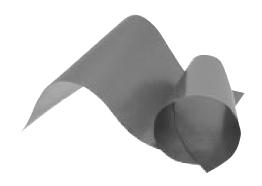
Panasonic

"PGS" Graphite Sheets

"PGS" Graphite Sheets

Type: **EYG**

PGS (Pyrolytic Graphite Sheet) is a thermal interface material which is very thin, synthetically made, has high thermal conductivity, and is made from a higly oriented graphite polymer film. It is ideal for providing thermal management/heat-sinking in limited spaces or to provide supplemental heat-sinking in addition to conventional means. This material is flexible and can be cut into customizable shapes.



Characteristics

| Characteristics S | | Specification | Specification | Specification |
|-------------------------|-------------------------------------|----------------------------------|----------------------------|----------------------------------|
| Thickness | | $0.10 \pm 0.03 \text{mm}$ | 0.07 ± 0.015 mm | 0.025 ± 0.010 mm |
| Densitv | | 0.85 a/cm ³ | 1.1 a/cm ³ | 2.1 a/cm ³ |
| Thermal conductivity | a-b plane | 600 to 800 W/(m·K) | 750 to 950 W/(m·K) | 1500 to 1700 W/(m·K) |
| Electrical conductivity | ity 10000 S/cm 10000 S/cm 20000 S/c | | 20000 S/cm | |
| Extensional strength | | 19.6 MPa 22.0 MPa 30.0 MPa | | 30.0 MPa |
| Expansion coefficient | a-b plane | $9.3 \times 10^{-7} \text{ 1/K}$ | 9.3 × 10 ⁻⁷ 1/K | $9.3 \times 10^{-7} \text{ 1/K}$ |
| | c axis | $3.2 \times 10^{-5} \text{ 1/K}$ | 3.2 × 10 ⁻⁵ 1/K | 3.2 × 10 ⁻⁵ 1/K |
| Heat resistance | | 400 °C | | |
| Bending(angle 180,R5 |) | 10000 cycles | | |

Design and specifications are each subject to change without notice. Ask factory for the current technical specifications before purchase and/or use. Should a safety concern arise regarding this product, please be sure to contact us immediately.

00 Sep. 2008

Sample Graphite Sheets

We have graphite sheets to be tested from 3 different companies.

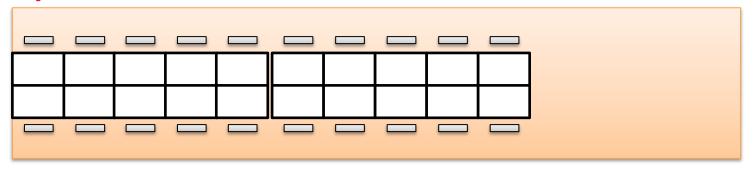
| Make | Panasonic | Kaneka | Blady |
|-----------------------------|-----------|--------|------------|
| Thickness [µm] | 70 | 40 | 70 |
| Thermal Conductivity [Wm/K] | 1000 | 500 | 300 ~ 1500 |



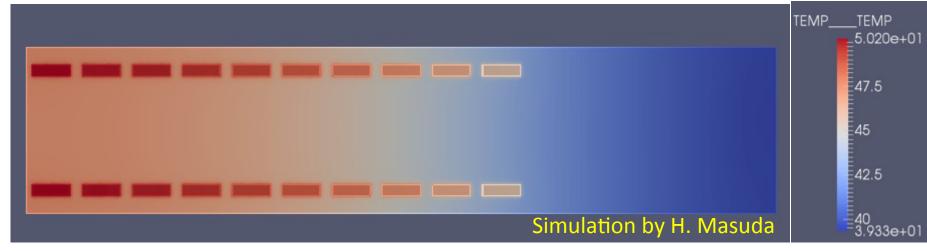
Dimension is made to be same with s0 HDIs ($30 \text{cm x } 4 \text{cm x } 70 \text{ } \mu\text{m}$)

Cooling Simulation

Layer-0



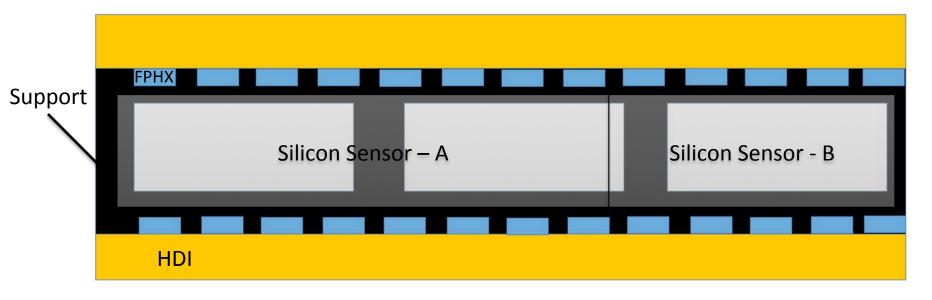
Predicted by the Simulation (Salome-meca Developed by Electricite De France)



Condition: FPHX 65mW/chip, $70\mu m$ Graphite Sheet (1200W/mK), 100% longitudinal heat transfer is assumed. Still need a fine tuning.

Reducing Material: Support

 Do we need to backup entire silicon acceptance or can it be open behind silicon sensors?



To be studied with engineers.

Improving Reconstruction Algorithm

Work by Gaku Mitsuka

- Alan's code does Hough transform for all MAPS, INTT, TPC. (Ignores multiple scattering effect).
- Step-1 (by mid Feb.) Hough transform only for TPC. Tracklet reconstruction by TPC only.
- Step-2 (by mid. March) Develop the algorithm to start from inner TPC tracklet to find relevant hit in INTT and MAPS. Search window reflects the multiple scattering effect.

Summary

- Due to the technical limit of HDI width, the ladder overlap between ladder will adds up material by factor of 2.
- HDI width is 38mm and unlikely to be narrower in future R&D.
- R&Ds are in progress for each components of ladders.
- Algorithm is under development to improve the tracking which makes the tracker material less impactful to the momentum resolution by taking into account the multiple scattering effect in the hit search window.

BACKUP

Silicon Module with Liquid/Air cooling Design

